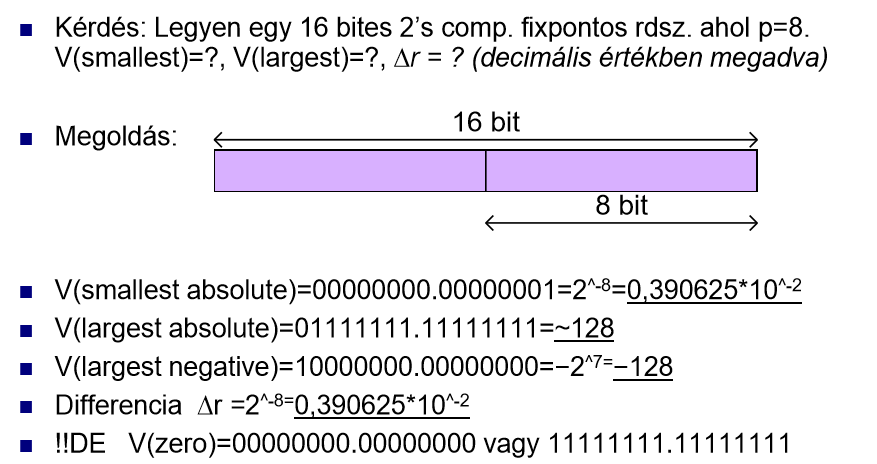
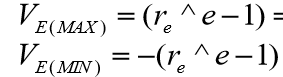
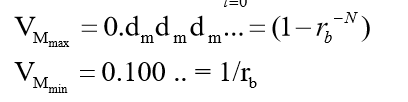
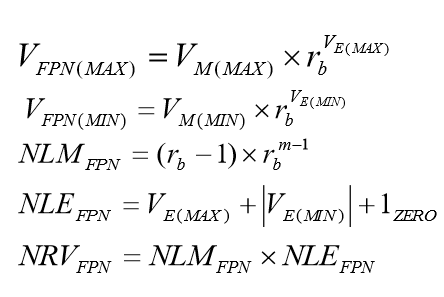
# Kettes komplemens feladat

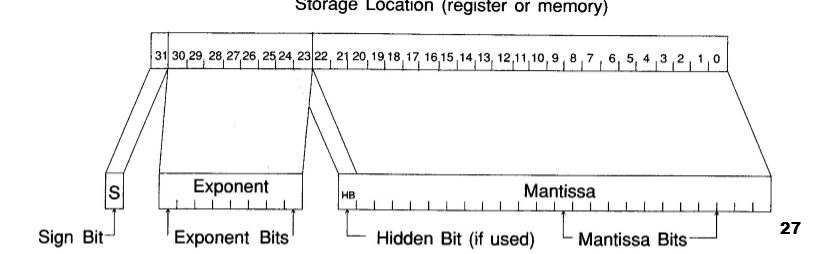


# Excess





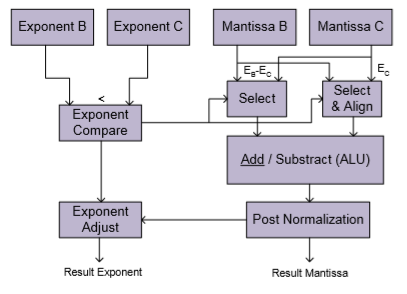
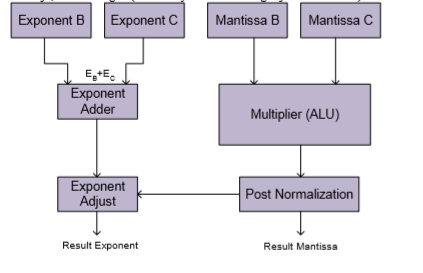
# IEEE



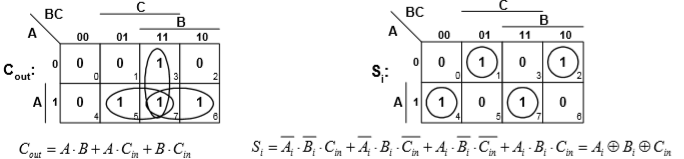
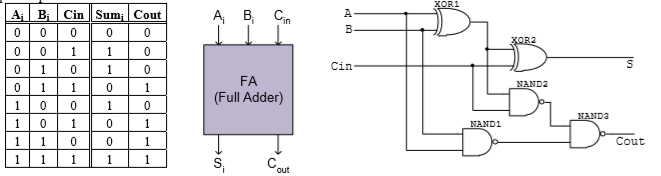
# VHDL

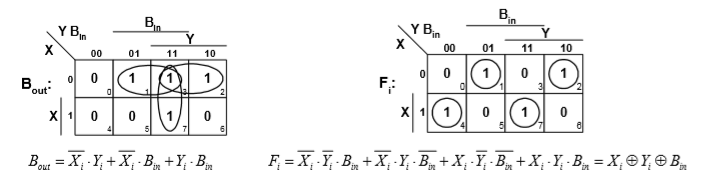
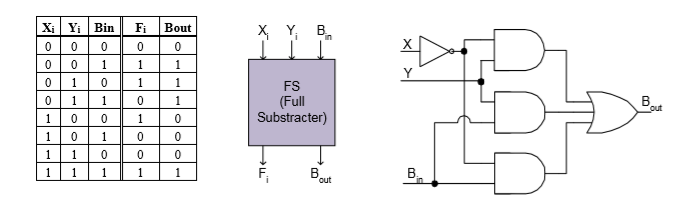
megy

# Lebegőpontos



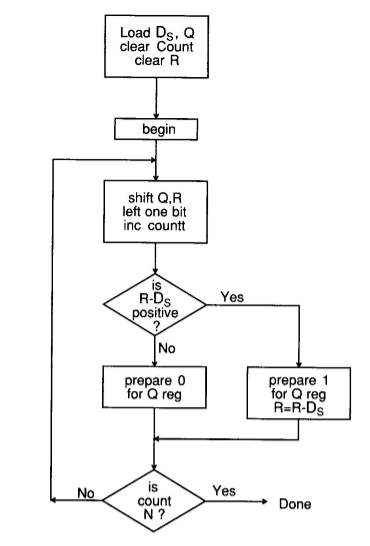
# FA, FS



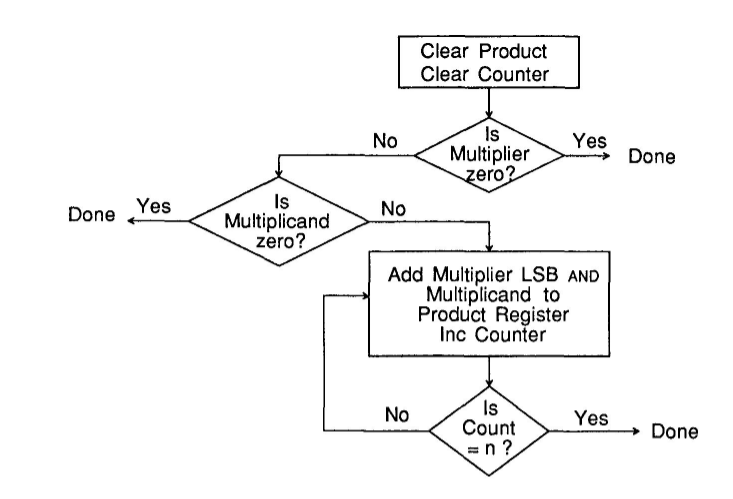


# Folyamatábrák

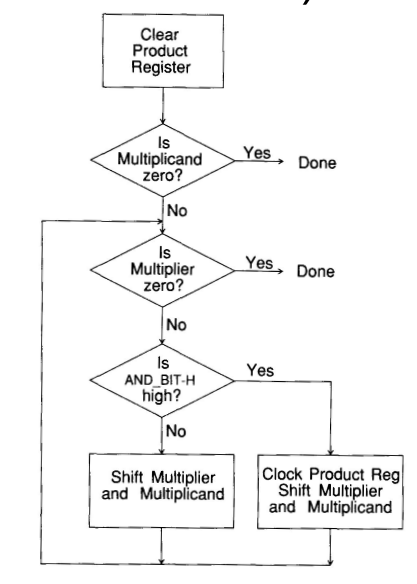
## osztó

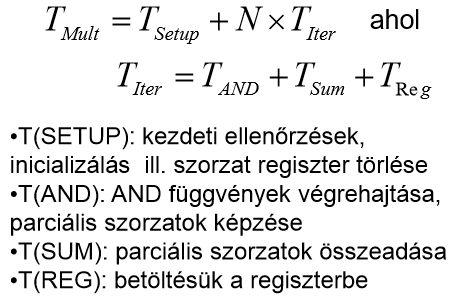


## shiftadd



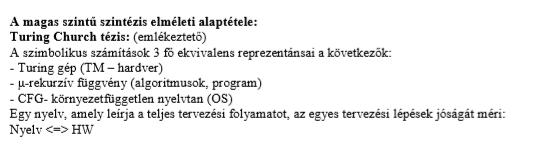
## Fordított sorrendű

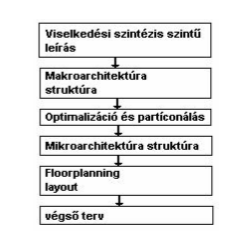


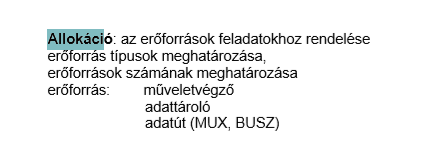


# Szintézis

HLS: High Level Synthesis: Magas-Szintű Szintézissel történő egységbe foglalás A HLS szinkron digitális rendszerek logikai szint feletti automatikus tervezését teszi lehetővé. Bemenete magas szintű hardver leíró nyelv (VHDL), amelynek segítségével a rendelkezésre álló adatbázisok alapján elektrom s áramköröket építhetünk.



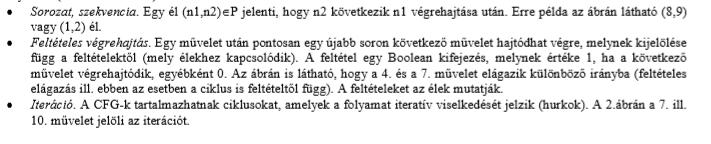


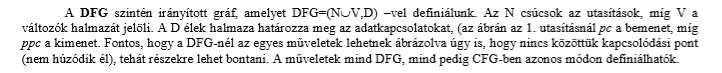




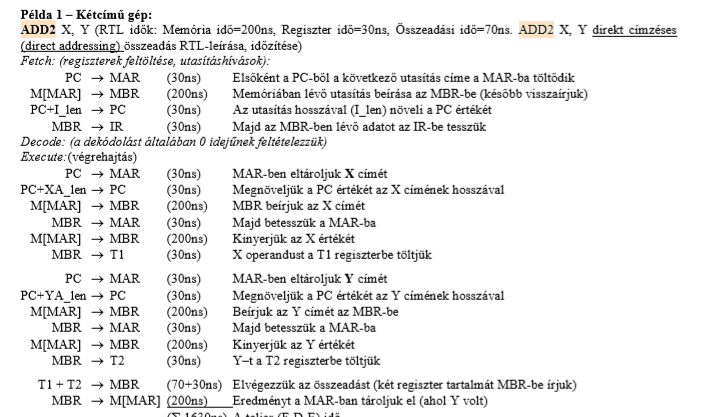
tervezés ütemezés

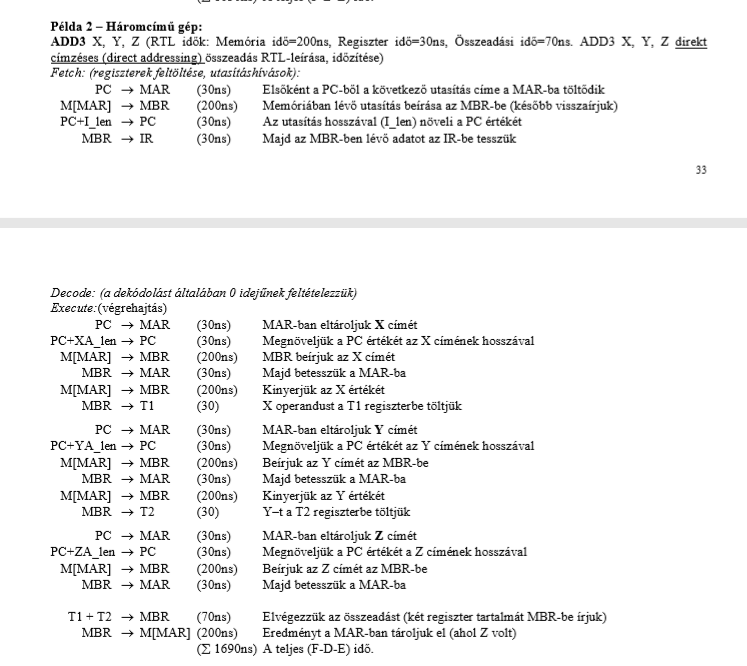


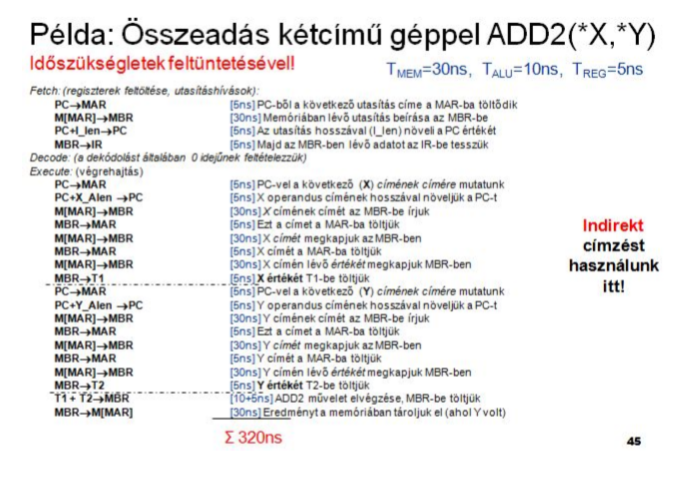




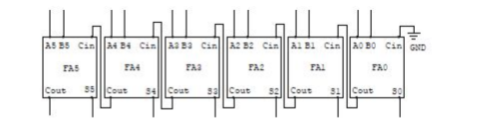
# Memória fos



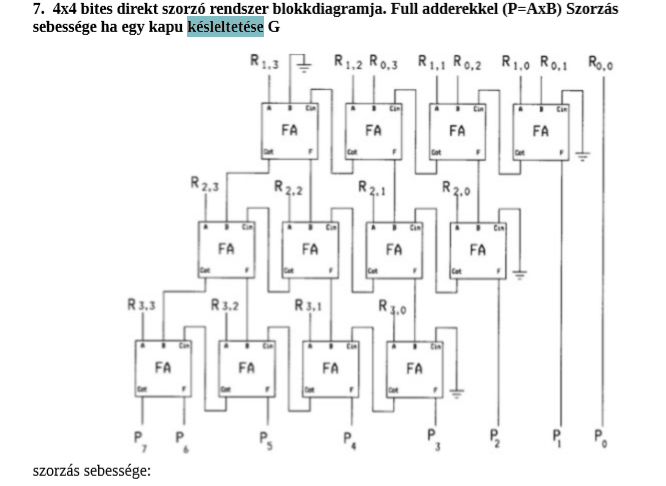


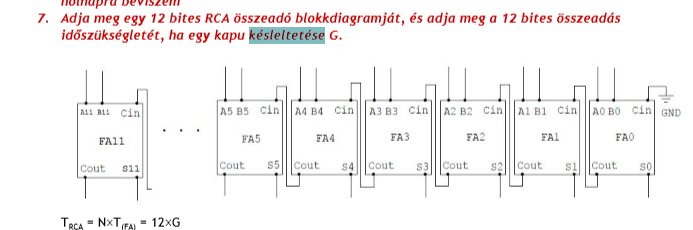
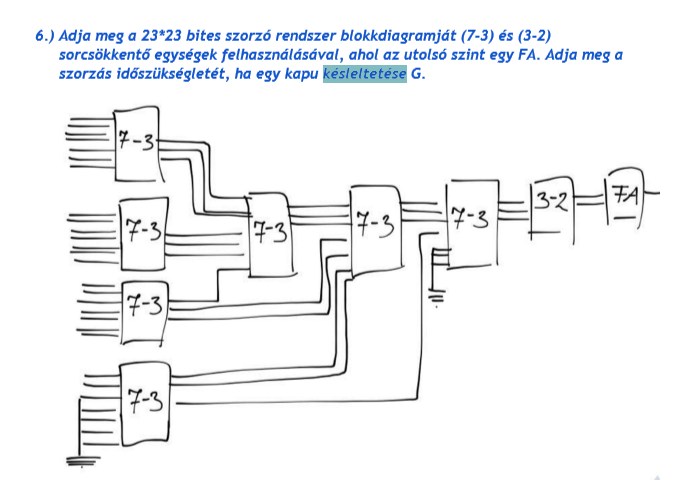
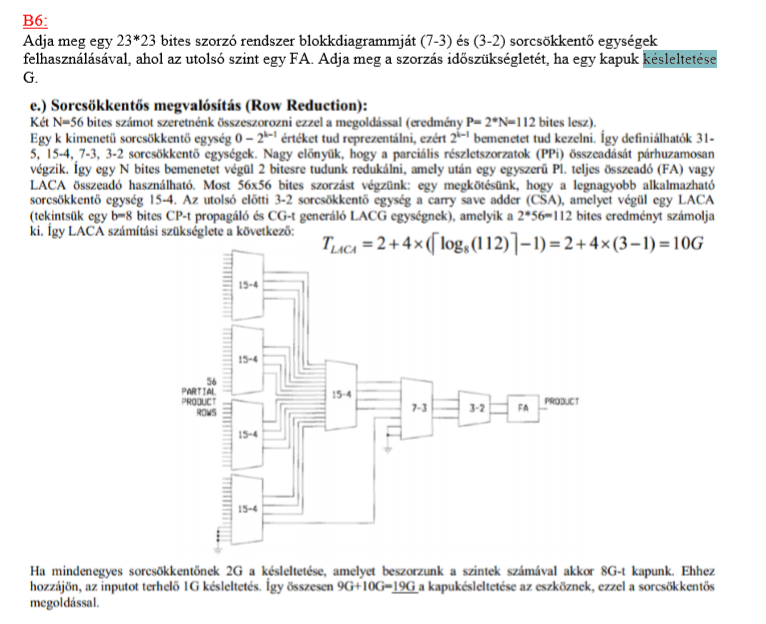


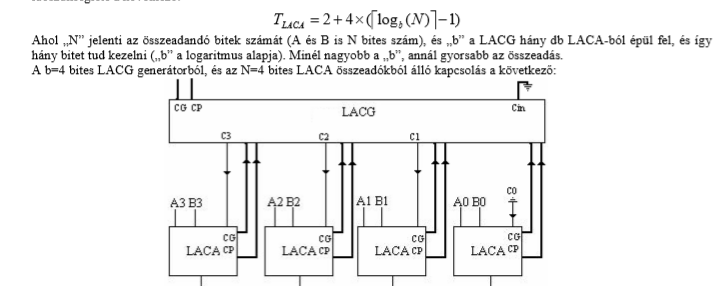
# RCA

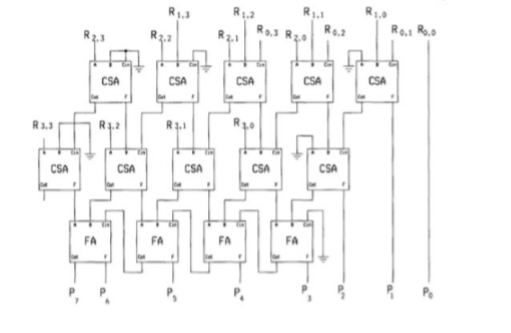


# Késleltetés G



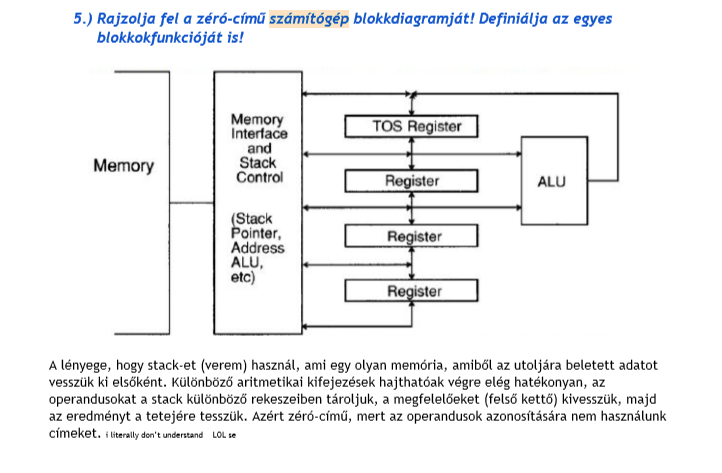


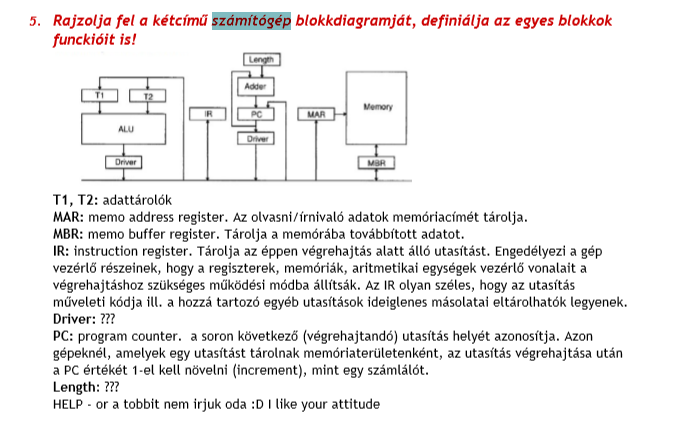


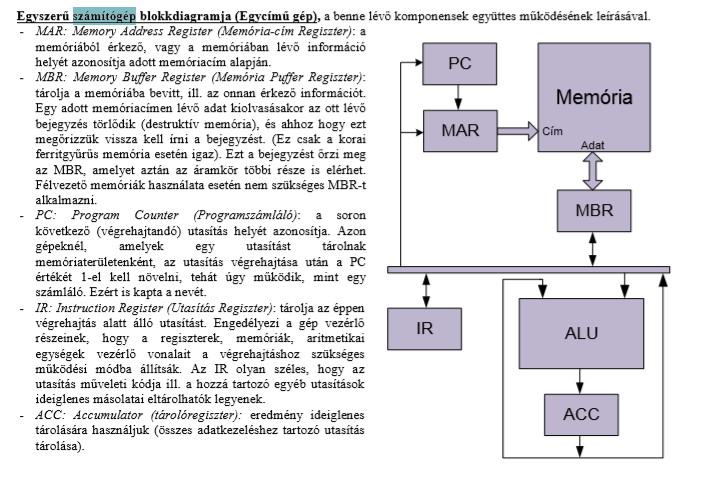


4x4 CSA-val

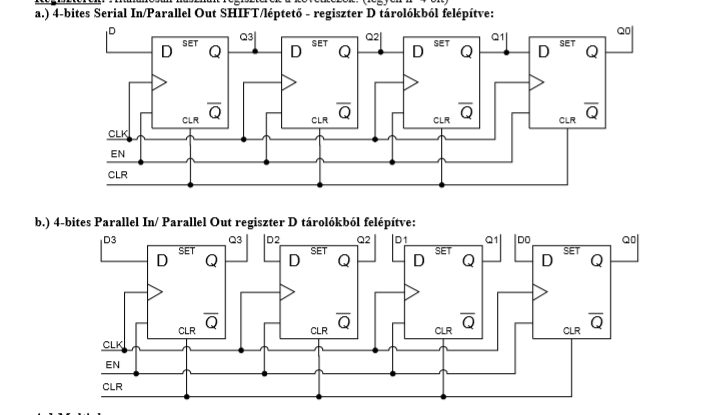
# Című számító



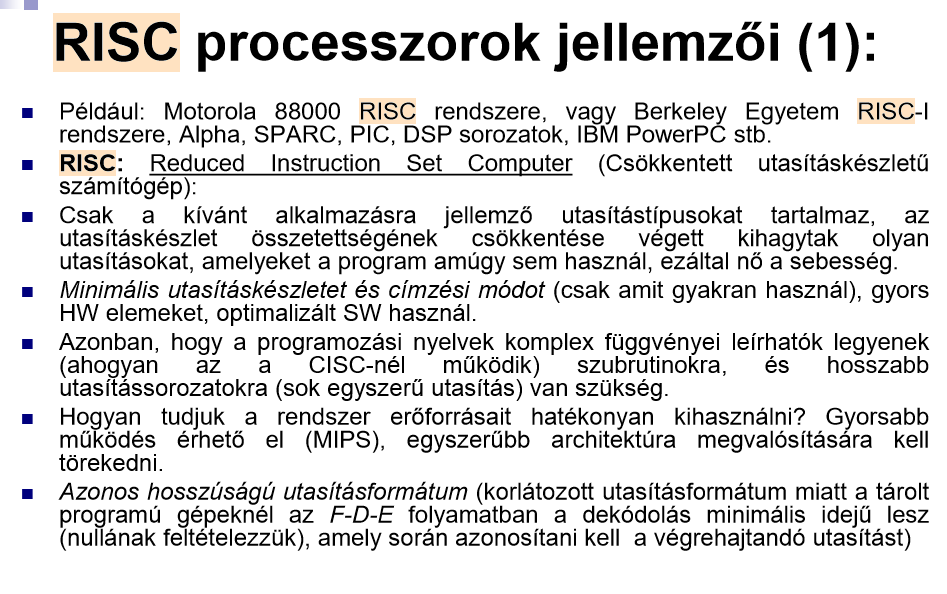


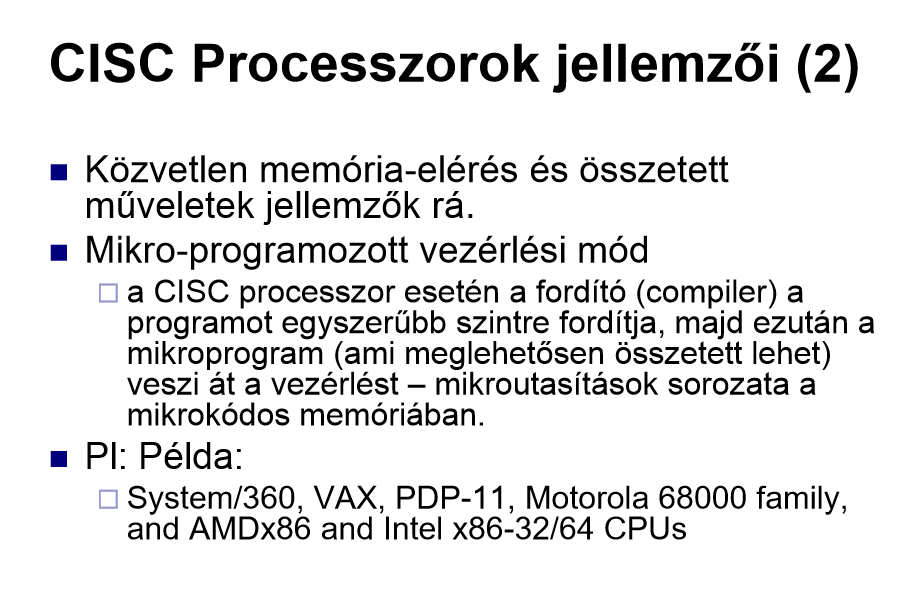
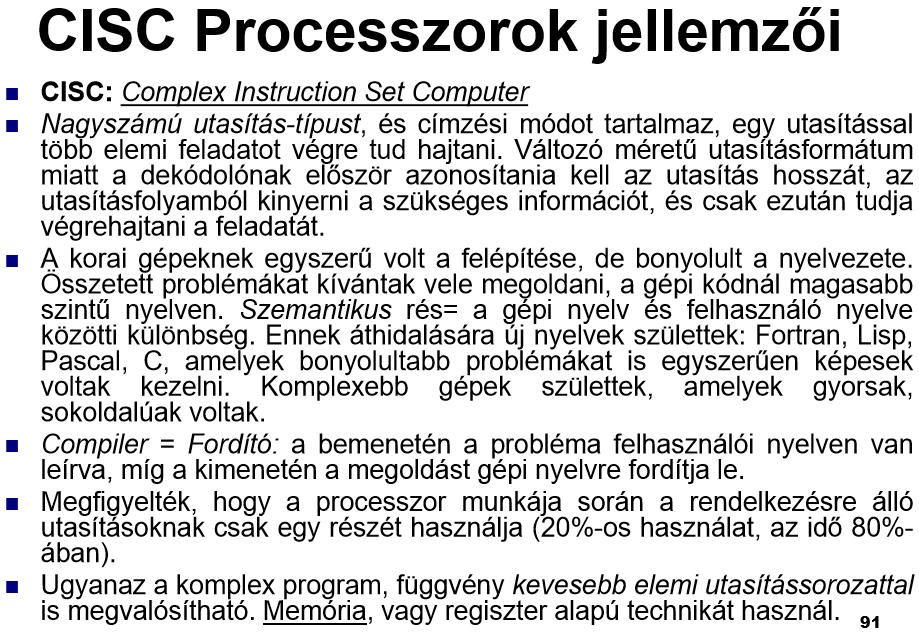


# D tárolós geci

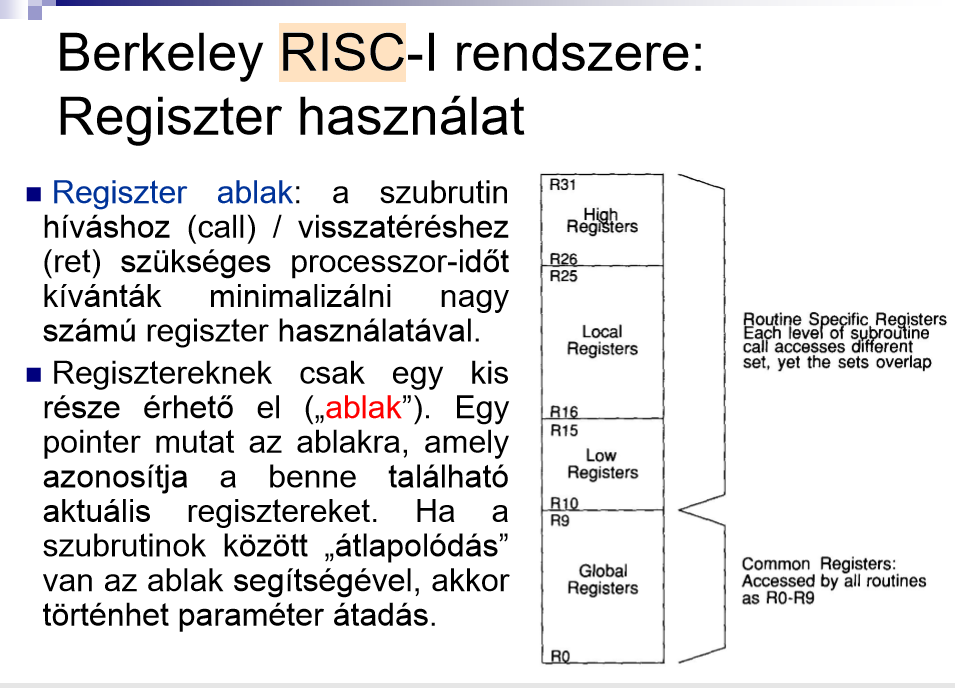


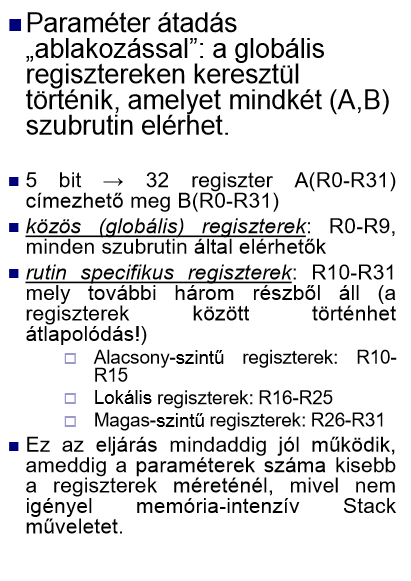
# RISC CISC



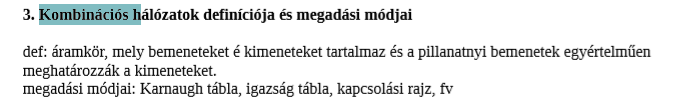


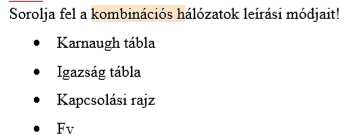
# Register ablakozás

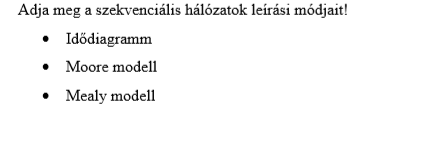


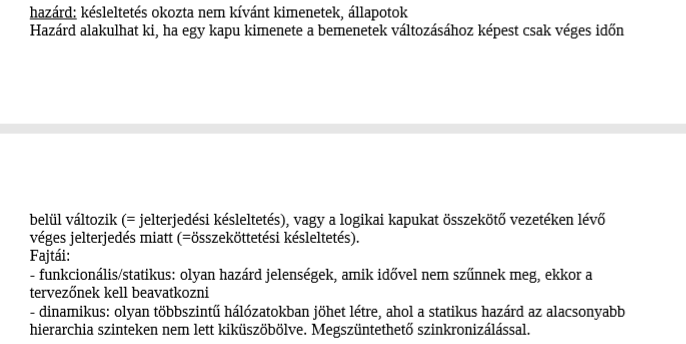
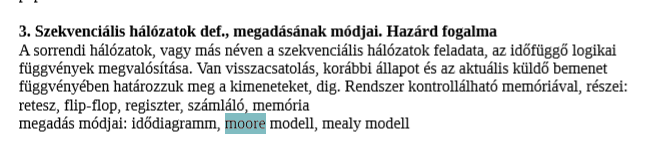


# Hálózatok









# ALU

