

A

Parallel architectures

1 ZH

2021. 11. 08.

1. Define the Rent rule (2)
2. Define the relationship of the signal delays on PCBs and on ICs, and give the explanation as well. (2)
3. To multiply two matrices by using systolic processor arrays draw the structure and the data stream as well. How many processors have to be used? (2)
Which kind of operation a processor doing? (0.5) Define the area and the time requirements? (0.5)
4. Define the analog computation model . Explain why can it be used for parallel computation. (2)
5. Define the parameters describing the computational complexity. (2)
6. Describe a fixed point DSP architecture, and define the function of the main blocks. Define the parts in the architecture supporting the parallel operation. (3)
7. Specify the time gain in pipeline operation. (2)
8. Define the bounds of pipeline operation. (2)
9. Effect of the Scaling Down to gate capacity and to the energy requirement (Figure+ explanation) (2)
10. Give the CNN model with the basic equations. (define the variables and the parameters), how can you define an elementary instruction? (3)
11. List the advantages of an open source ISA (RISC-V) over commercial ISAs (x86, ARM) (2)